ISP SOC XC7022

1080p@30fps
720p@60fps

2M
HDR
WDR

MIPI 2 TX
960M bps
MIPI 2 RX
960M bps
I2C slave host
I2C master
I2C host
PLL 6 27M
1.8V/2.8V/3.3V IO
-20 C~ 70 C
Sleep/Active
0.4mm pitch 5x5 QFN40

QFN5x5-40L

XC7022
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XC7022
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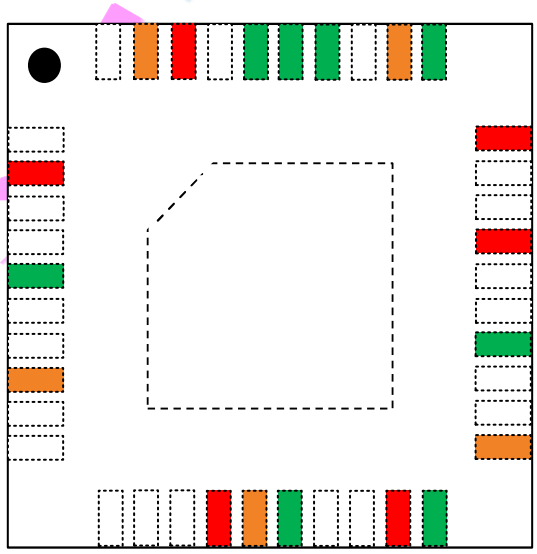

1 XC7022 ( )

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XC7022 32 RISC ISP SoC

1080P RAW

YUV MIPI Smart AE XC7022

8/10bit RAW YUV422 1080P@30fps 720@60fps

1.1

XC7022

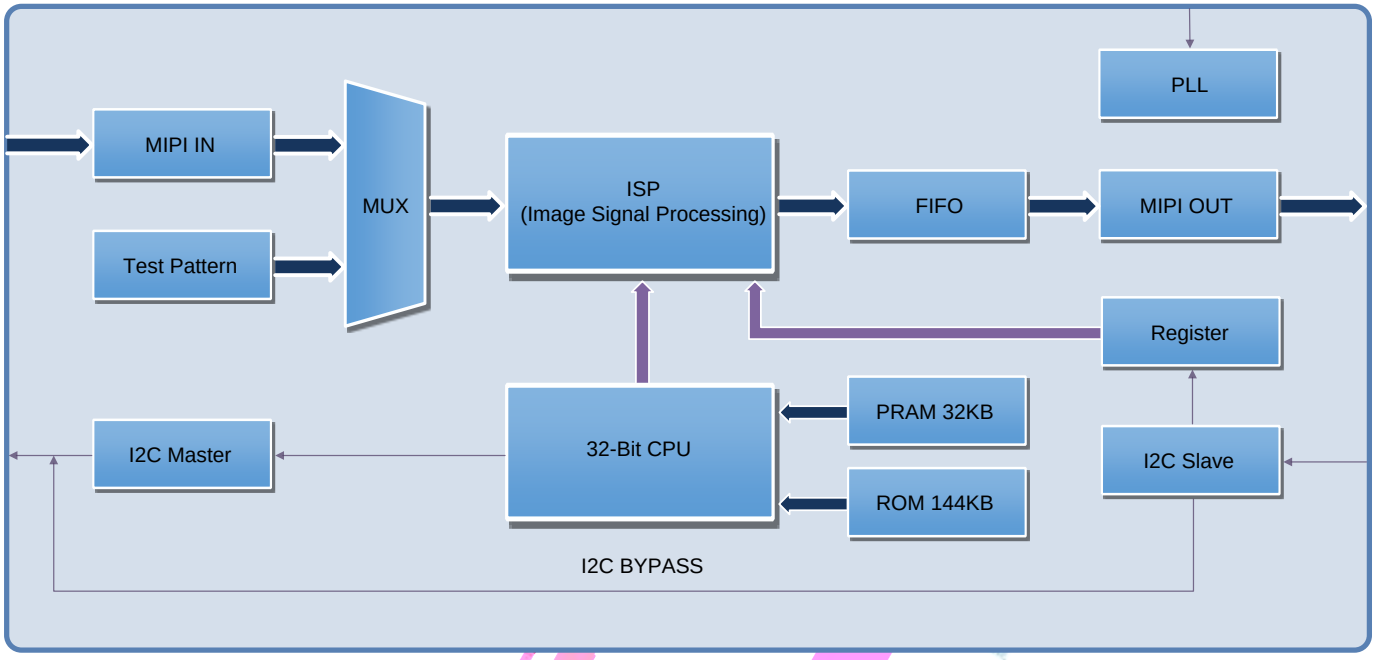
1 XC7022

No.	signal Name	pad type(1)	description	
1	SCK2	I/OD	I2C Clock (Host)	Host
2	EVDDRX	P	MIPI RX digital power Supply 1.2V	MIPI RX Power Domain (Sensor)
3	RXDN1	I DS	MIPI RX data lane 1 negative input	
4	RXDP1	I DS	MIPI RX data lane 1 positive input	
5	EGND	G	MIPI RX analog ground	
6	RXCN	I DS	MIPI RX clock lane negative input	
7	RXCP	I DS	MIPI RX clock lane positive input	
8	PVDD33_RX	P	MIPI RX Analog Power Supply 1.8V /2.8V/3.3V	
9	RXDN0	I DS	MIPI RX data lane 0 negative input	
10	RXDP0	I DS	MIPI RX data lane 0 positive input	
11	CCLK	O	Sensor Referenced Clock	Sensor Power Domain
12	SDA0	I/OD	I2C Data (Sensor)	
13	SCK0	I/OD	I2C Clock (Sensor)	
14	CVDD	P	Digital Core Power Supply 1.2V	
15	PADVDD1	P	I/O Group1 Power Supply 1.8V /2.8V/3.3V	
16	VSS	G	GROUND	
17	SPWDN	O	Sensor Power-Down Control 1: Power down mode 0: Normal mode	
18	SRESET	I/O	Sensor Reset Control	
19	CVDD	P	Digital Core Power Supply 1.2V	
20	VSS	G	GROUND	
21	AVDD33_TX	P	MIPI TX Analog Power Supply 1.8V /2.8V/3.3V	MIPI TX Power Domain (Host)
22	TXDP0	O DS	MIPI TX data lane 0 positive output	
23	TXDN0	O DS	MIPI TX data lane 0 negative output	
24	EGND	G	MIPI TX analog ground	

No.	signal Name	pad type(1)	description	
25	TXCP	O DS	MIPI TX clock lane positive output	
26	TXCN	O DS	MIPI TX clock lane negative output	
27	EVDDTX	P	MIPI TX digital power Supply 1.2V	
28	TXDP1	O DS	MIPI TX data lane 1 positive output	
29	TXDN1	O DS	MIPI TX data lane 1 negative output	
30	CVDD	P	Digital Core Power Supply 1.2V	Host Power Domain
31	VSS	G	GROUND	
32	PADVDD2	P	I/O Group2 Power Supply 1.8V /2.8V/3.3V	
33	RESETB	I	System Reset; (active low with internal pull-up resistor) 1: Normal mode 0: Reset mode	
34	VSS	G	GROUND	
35	VSS	G	GROUND	
36	VSS	G	GROUND	
37	XMCLK	I	PLL Master Reference Clock Input	
38	CVDD	P	Digital Core Power Supply 1.2V	
39	PADVDD2	P	I/O Group2 Power Supply 1.8V /2.8V/3.3V	
40	SDA2	I/OD	I2C Data (Host)	

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input and Output Signal, D = Open drain, DS = Differential

1.2 XC7022



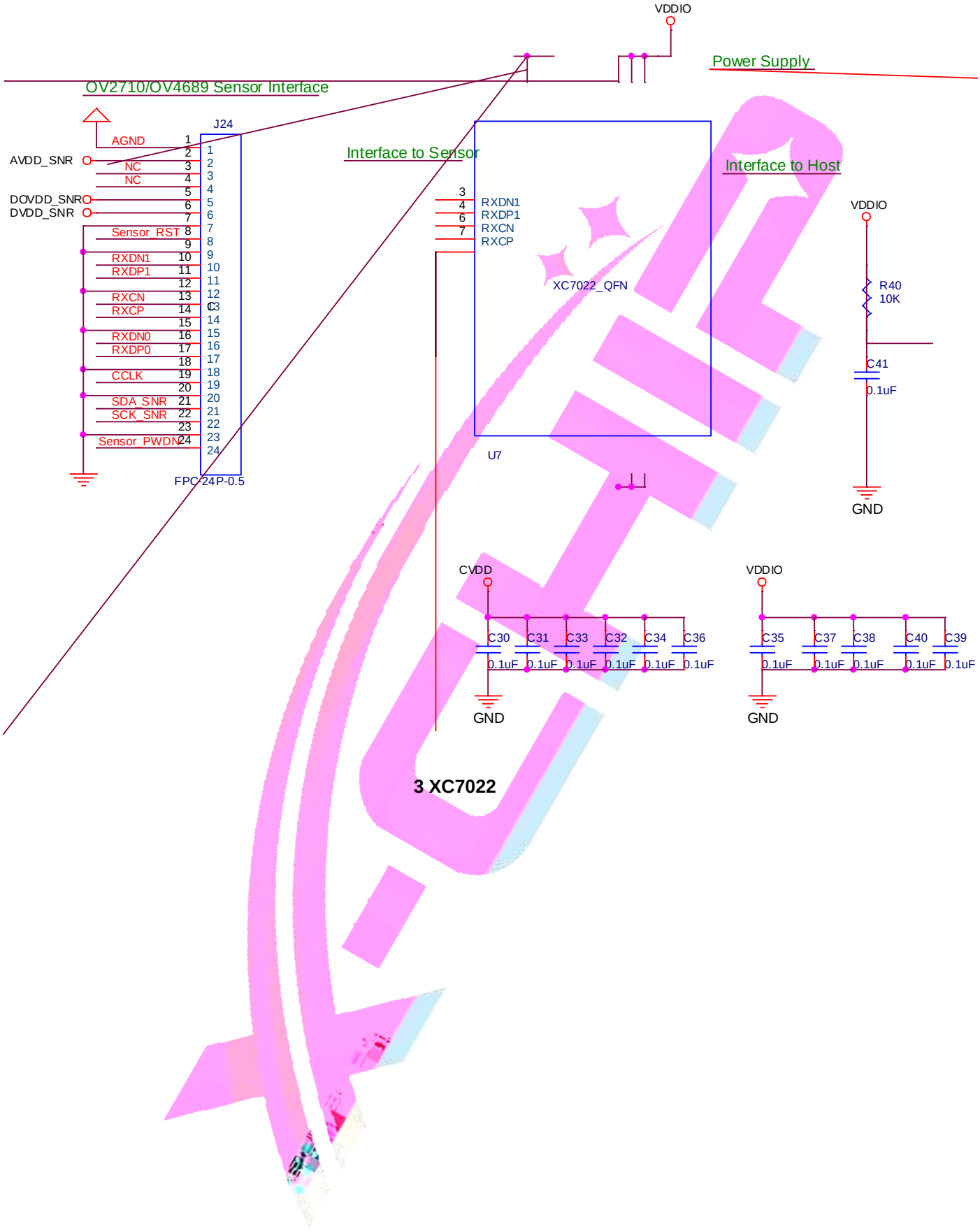
2 XC7022

1.3

			RoHS	
XC7022QNR	-20 70	QFN40, 5mmx5mm		

1.4

XC7022 1080P MIPI MIPI RX RAW
MIPI TX HOST FAE fae@x-chip.cn


VDDIO
Power Supply
OV2710/OV4689 Sensor Interface
J24
AGND
AVDD_SNR
NC
NC
DOVDD_SNR
DVDD_SNR
Sensor_RST
RXDN1
RXDP1
RXCN
RXCP
RXDN0
RXDP0
CCLK
SDA_SNR
SCK_SNR
Sensor_PWDN
FPC-24P-0.5
Interface to Sensor
RXDN1
RXDP1
RXCN
RXCP
XC7022_QFN
U7
Interface to Host
VDDIO
R40
10K
C41
0.1uF
GND
CVDD
C30
C31
C33
C32
C34
C36
0.1uF
GND
VDDIO
C35
C37
C38
C40
C39
0.1uF
GND

3 XC7022

2.1

2

PADVDD1	Sensor PAD	-0.5	TBD(3.6)	V
PADVDD2	Host PAD	-0.5	TBD	V
PVDD33_RX	MIPI RX PAD	-0.5	TBD	V
AVDD33_TX	MIPI TX PAD	-0.5	TBD	V
CVDD	Core	-0.5	TBD(2.0)	V
EVDDRX	MIPI RX Core	-0.5	TBD	V
EVDDTX	MIPI TX Core	-0.5	TBD	V
Tstg		-55	+150	
Ta		-20	+70	

3

PADVDD1	Sensor PAD	2.52/2.97	2.8/3.3	3.08/3.6	V
PADVDD2	Host PAD	2.52/2.97	2.8/3.3	3.08/3.6	V
PVDD33_RX	MIPI RX PAD	2.52/2.97	2.8/3.3	3.08/3.6	V
AVDD33_TX	MIPI TX PAD	2.52/2.97	2.8/3.3	3.08/3.6	V
CVDD	Core	1.08	1.2	1.32	V
EVDDRX	MIPI RX Core	1.08	1.2	1.32	V
EVDDTX	MIPI TX Core	1.08	1.2	1.32	V

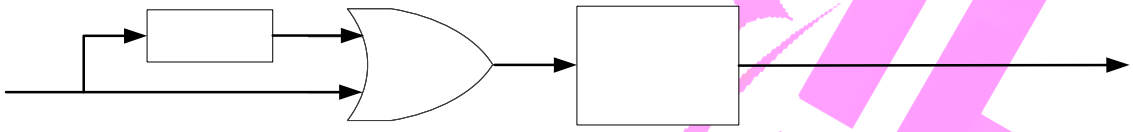
2.2

4

TCT	TC1000(-65 ~150 ,1000Cycles)		TBD
HAST	UHAST96(130 , 85%RH, 33.3 PSIA, 100% Bias, 96Hours)		TBD
MSL	MSL3(3Cycles)		TBD

3.1

3.1.1



4

XC7022 RESETB

4 1.2V

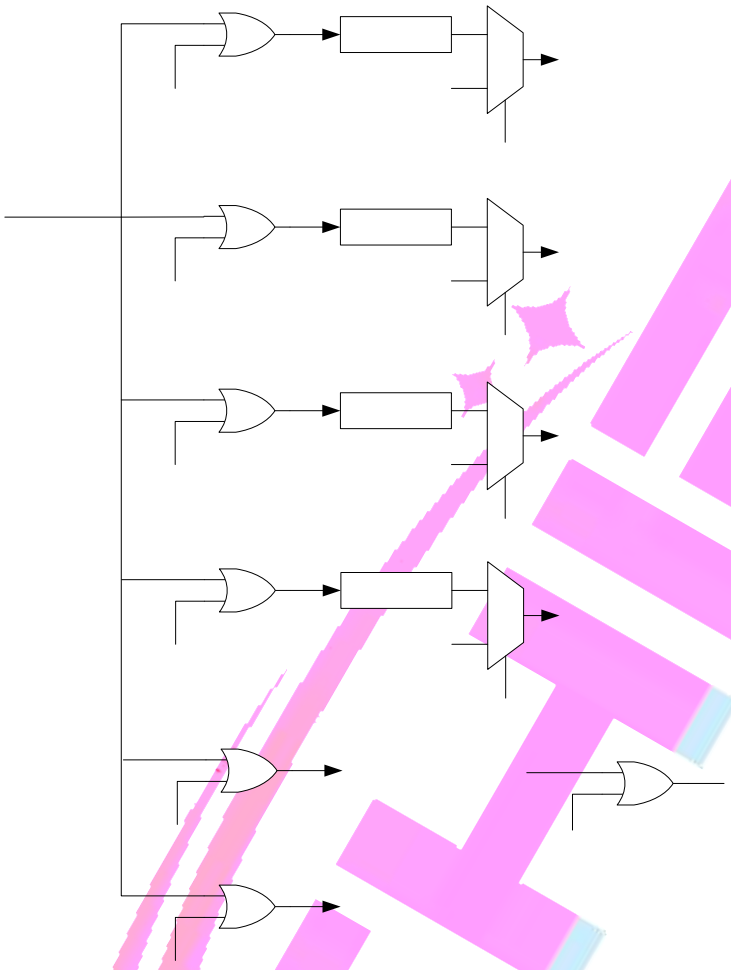
1.2V

3.1.2

CPU RST HOST I2C RST RST

0x80500018 bit

3.1.3 XC7022



5 XC7022

3.3 ISP

6 XC7022

上电过程：

1 Host CVDD EVDD PADVDD1 PADVDD2 PVDD33 AVDD33

2 XC7022 RESETB

3 Host XC7022 XMCLK

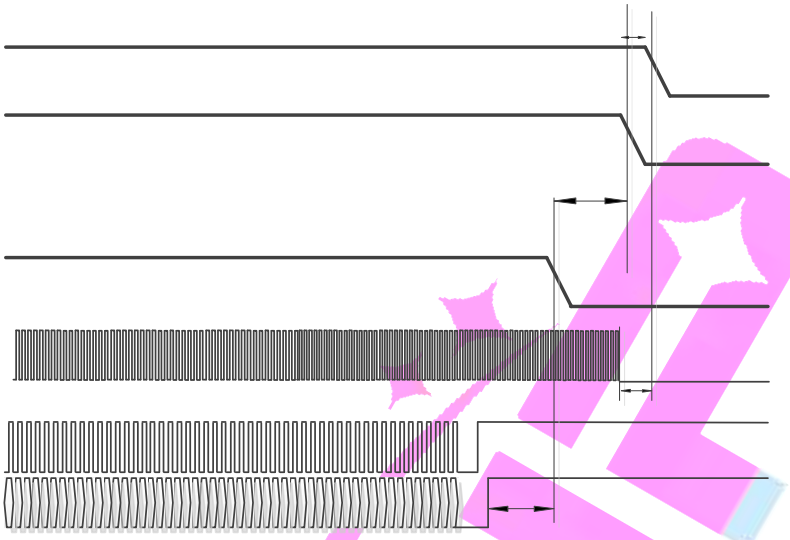
4 RESETB 25ms Host I2C Slave

5 XC7022 I2C master sensor sensor

6 XC7022

3.4 ISP

ISP sensor



7 XC7022 sensor

下电过程：

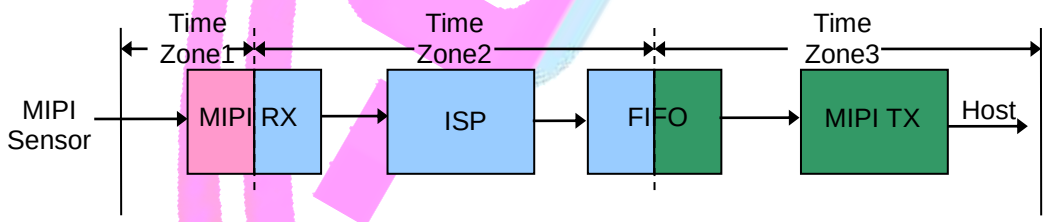
1 Host XC7022 I2C

2 2.5ms RESETB

3 RESETB XMCLK

4 CVDD EVDD PADVDD PVDD33 AVDD33

3.5



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1 MIPI RX 1

2 2

3 MIPI TX 3.

4.1 PLL

MIPI TX PHY MIPI TX PHY

960MHz 120Mhz

4.2 MIPI TX PHY

MIPI TX PHY MIPI TX (clock lane)

(data lane)

4.2.1

1

2 960M bps

3 120M

4.3 MIPI RX PHY

CMOS MIPI RX (clock lane) (data lane)

4.3.1

1

2 960M bps

3 120M

5.1 MIPI

MIPI MIPI MIPI
960M / MIPI RAW8/RAW10 YUV422

1 RAW8/RAW10/YUV422
2 960Mbps
3
4 ECC CRC
5
6 1-bit
7 2
8 FIFO
9

5.2 MIPI

MIPI MIPI . MIPI
RAW8/RAW10 YUV422

5.3 I2C

ISP I2C CPU sensor I2C SCK SDA
2.2K~10K PADVDD I2C IO PADVDD

5.3.1

1 I2C slave host
2 I2C master
3 I2C host host
4 Standard/Fast 400kbps

I2C slave 36H

5.3.2 I2C Slave

CPU I2C slave SCK1 SDA1 ISP
I2C bypass CPU I2C Sensor ISP 32
I2C 16 ISP 2 16 0xFFFD
ADDR[31:24] 0xFFFE ADDR[23:16] page
0x80300001 I2C 0xFFFD 0x80 0xFFFE 0x30
I2C 0x0001 page 0xFFFD 0xFFFE page
Host CPU I2C master ISP I2C slave
16 8

CPU ISP

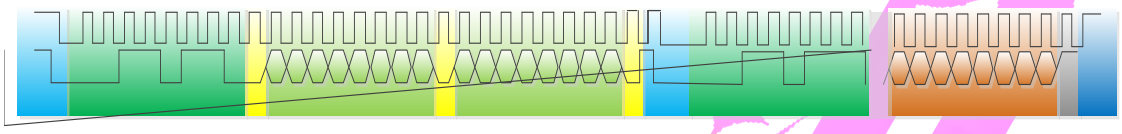
1. Master START
2. Master I2C Slave ID 0x36 ACK
3. Slave ACK
4. Master Reg 8 Register ADDR[15:8] ACK
5. Slave ACK
6. Master Reg 8 Register ADDR[7:0] ACK
7. Slave ACK
8. Master Data 8bit ACK
9. Slave ACK
10. Master STOP

9 I2C slave

CPU ISP

1. Master START
2. Master I2C Slave ID 0x36 ACK
3. Slave ACK
4. Master Reg 8 Register ADDR[15:8] ACK
5. Slave ACK
6. Master Reg 8 Register ADDR[7:0] ACK

7. Slave ACK
8. Master I2C 0x37 ACK
9. Slave ACK
10. Slave Data 8bit
11. Host STOP



10 I2C slave

5.3.3 I2C Master

ISP I2C master I2C ISP master sensor slave

ISP I2C master 8 8 16 16 16
8 I2C slave

5.4

RISC

5.4.1

4~16 RGB

5.4.2

Lens Shading Correction

5.4.3

Defective Pixel Correction DPC

5.4.4

Auto Exposure AE Gain Control

XC7023

5.4.5

RAW YUV

5.4.6

Automatic White

Balance AWB

5.4.7

XC7022 25

XC7022 VCM

5.4.8

RAW Bayer RGB RAW RGB
RGB

5.4.9

( ) De-noise

5.4.10

Sensor RAW RGB Bayer Pattern R G B
Color Interpolation RAW RGB
RGB RAW RGB data RGB data

5.4.11

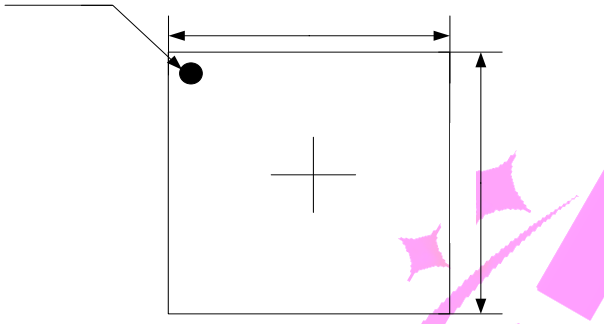
(Color Matrix)

R G B R G B

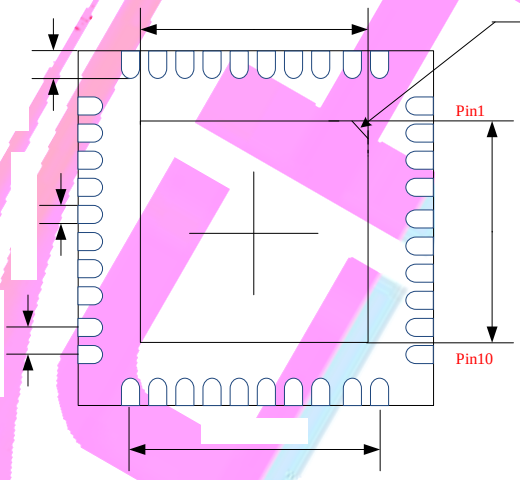
5.4.12 Gamma

XC7022 Gamma RAW RGB Gamma
XC7022 Gamma 64

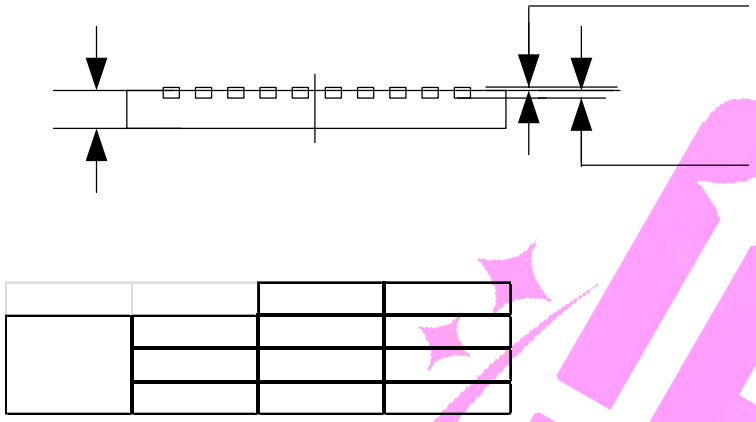

X-CHIP



11 XC7022



12 XC7022



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Note: TSLP and SLP share the same expose outline but with different thickness.

XC7022 uses TSLP.